REMARKS

Claims 1 to 26 are pending in this application of which claims 1, 8, 9, 10 and 15 are the independent claims. Favorable reconsideration and further examination are respectfully requested.

Initially, Applicant thanks the Examiner for the indication that claims 4 and 7 contain allowable subject matter. In response to this indication, Applicants have added additional claims. Independent claim 10 includes the limitations of claim 4 and independent claim 15 includes the limitations of claims 6 and 7. Applicants submit that claims 10 and 15 and their dependent claims are allowable.

Claims 1, 2, 5, 6, 8 and 9 were rejected under 35 U.S.C. §102 over McDysan (U.S. Patent 6,226,260); and claim 3 was rejected under §103 as being obvious over McDyson in view of PCI Local Bus Specifications. As shown above, Applicant has amended the claims to define the invention more clearly. In view of these amendments, withdrawal of the art rejection is respectfully requested.

Claim 1, as amended, is directed to a device for converting data sequences between frame relay (FR) format and asynchronous transfer mode (ATM) format. The device includes an FR communication module for connecting to at least one FR communication link, an ATM communication module for connecting to an ATM communication link and a central computer for controlling the FR communication module and the ATM communication module. The device also includes a buffer memory, which is connected via an internal communication link to the central computer, the FR communication module and the ATM communication link. The buffer

memory is configured to store FR data sequences from the FR communications module and ATM data sequences from the ATM communications module.

The applied art is not understood to disclose or to suggest the foregoing features of claim 10. In particular, McDysan does not disclose or suggest a buffer memory that is configured to store FR data sequences from the FR communications module and ATM data sequences from the ATM communications module.

In this regard, McDysan shows a processor 1020, a universal asynchronous receiver/transmitter (UART) 1010, a FR/ATM adapter 1040 and a memory 1030 all connected by a bus 1015. The memory 1030 includes a T/R FR UNI table 1035 (See FIG. 10 of McDysan). An incoming FR data frame 1201 includes an FR Data Link Connection Identifier (DLCI) header and a data information field I (data I). Processor 1020 uses the DLCI header to index T/R FR UNI table 1035 to find an appropriate ATM header as a prefix to data I. McDysan's device also uses table 1035 to save status messages of each active DLCI header; however, these status messages are not part of the FR data sequence. Furthermore, data I is never saved in memory 1030. (see column 10 lines 25 to 65 of McDysan).

When an ATM cell is received, the ATM cell includes data I along with ATM VCC and ATM DLCI fields. The ATM VCC and ATM DLCI fields are used to index table 1035 to find the appropriate FR DLCI header to include with data I. Processor 1020 stores a Rx ATM PHY value, but this value is not part of the received ATM cell. Again, data I is never stored in memory 1030 (see column 10 line 66 to column 11, line 31).

Therefore, McDysan does not disclose or suggest a buffer memory that is configured to store FR data sequences from the FR communications module and ATM data sequences from the ATM communications module.

The noted distinctions are not trivial, but represent a significant inventive step, as will be appreciated by those in the telecommunications industry. As disclosed by the Applicant in the specification, storing data sequence in a buffer memory, instead of a computer memory, increases the data throughput because the computer is not interrupted during reading in or reading out a data sequence (see page 2, line 26 to page 3, line 6 of the Applicant's specification). To the contrary, McDysan's device reads in a data sequence and performs the conversion of the data sequence by finding the appropriate headers. Thus, McDysan's device is interrupted from receiving additional data sequences until the conversion is complete because McDyson never stores the data sequences in a buffer memory.

For at least the reasons indicated above, claim 1 is believed to be allowable.

Claims 8 and 9 are method claims that roughly correspond to claim 1; and, therefore, claims 8 and 9 are believed to be allowable for at least the same reasons noted above with respect to claim 1.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as

an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing amendments and remarks, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

All correspondence should be directed to the above address. Applicant's attorney can be reached by telephone at the number shown above.

Enclosed is a $280 check for excess claim fees and a $110 check for the One-Month Extension fee. No other fee is believed to be due for this Amendment; however, if any fees are due, please apply such fees to Deposit Account No. 06-1050 referencing Attorney Docket 12758-060US1.

Respectfully submitted,

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